Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**End Semester Examination – Nov/Dec – 2018**

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| **Code :** | **18EC3029** | **Duration :** | **3hrs** |
| **Sub. Name :** | **ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS** | **Max. marks :** | **100** |

**ANSWER ANY FIVE QUESTIONS (5 x 16 = 80 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | Analyse the operation of Common-Drain stage using MOSFET. Examine the input-output characteristics and calculate the small signal gain with a small signal equivalent circuit. | CO1 | 12 |
| b. | With diagrams, explain the significance of a folded cascode stage. | CO1 | 4 |
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| 2. | a. | Interpret the Common-Mode response of the differential pair and infer the CM gain. | CO2 | 6 |
| b. | Illustrate the Large signal analysis of the Differential pair with active current mirror and realistic current source. | CO2 | 10 |
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| 3. |  | Evaluate the transfer function of the Common-Source stage using Miller's effect. Justify the stability of the CS stage for various frequency ranges. | CO3 | 16 |
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| 4. | a. | Explain the effect of loading in Current-Voltage feedback network using Z model. | CO4 | 10 |
| b. | Summarize the properties of feedback circuits. | CO4 | 6 |
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| 5. | a. | Determine the input common mode voltage range and closed loop output impedance for cascode op-amp. | CO5 | 8 |
| b. | List the various factors that limit the slew rate of opamps and discuss any one method for improving the same. | CO5 | 8 |
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| 6. |  | Analyze the frequency response of the following amplifiers.   1. Differential Pair. 2. Single stage amplifier with active load. | CO2 | 16 |
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| 7. |  | Discuss the types of noises available in the integrated circuits. Calculate the total output noise voltage of the given circuit. | CO3 | 16 |
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| **COMPULSORY QUESTION (1 x 20 = 20 Marks)** | | | | |
| 8. | a. | Examine the need for frequency compensation in operational amplifiers. | CO6 | 10 |
| b. | Explain the basic PLL topology with necessary diagrams. Implement a simple PLL in CMOS technology. | CO6 | 10 |